REMARKS

This Amendment seeks to place this application in condition for allowance. Claims 151-195 are pending, and claims 189-195 are allowed. Several of the pending claims have been amended to improve clarity and/or correct for minor typographical errors. All of the Examiner's rejections have been addressed. No new matter has been added.

OFFICE ACTION

In the Office Action mailed May 21, 2002 (hereinafter, "the OFFICE ACTION"), independent claims 189-195 were found to be allowable.

In addition, independent claims 151, 166, 173 and 182, and certain claims which depend therefrom, were rejected under 35 USC 102(a) as being anticipated by what the Examiner refers to as "admitted prior art". Further, the remaining claims were objected to as being dependent upon a rejected base claim, but were found to be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Each rejection is addressed separately below.

35 USC 102(a) Rejection

In the OFFICE ACTION, independent claims 151, 166, 173 and 182, and certain dependent claims, were rejected under 35 USC 102(a) as being anticipated by "applicant's admitted prior art". (OFFICE ACTION, pages 2 and 3, item 2). It is respectfully

submitted that those rejected claims present patentable subject matter.

In the OFFICE ACTION, the examiner refers to the "admitted prior art" as "for example col. 10 of U.S. Pat. No. 5,638,334... wherein the operation of 'conventional DRAMs' is explained with regard to how precharging is done and controlled". Applicants submit that this is nothing more than a reference to conventional asynchronous dynamic random access memory devices ("DRAMs", hereinafter, "conventional DRAM devices" or "conventional DRAMs"). (See, for example, U.S. Patent 5,638,334, col. 10, lines 15-18 and 21-24).[1] The reasons why such conventional DRAMs do not anticipate the claimed subject matter is discussed in additional detail below.

The Examiner correctly recognizes that the objected to claims 153-156, 159, 163-165, 167, 171, 180, and 191 present patentable subject matter. Applicants further assert that, although not separately addressed herein, dependent claims 152, 157, 158, 160-162, 168-170, 172, 174-179 and 183-188 also incorporate limitations that present patentable subject matter in their own right. However, to present a more concise response to the OFFICE ACTION, only certain limitations or elements of independent claims 151, 166, 173, and 182 are discussed below. No inference or conclusion of any kind should be drawn from the absence of comments pertaining

[1] Because the Examiner referred to U.S. Patent 5,638,334 in the OFFICE ACTION (See, page 2, item 2), Applicants also make reference to U.S. Patent 5,638,334 -- a patent based on the same ancestor application as the instant application.

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to other limitations or elements, whether those limitations or elements are contained in independent or dependent claims.

Applicants address the rejection to each of the independent claims separately below.

Claim 151 is not anticipated USC 35 USC 102(a)

Claim 151 is directed to a synchronous integrated circuit device having a memory array and including, in part, "a plurality of input receivers to sample an operation code synchronously with respect to the external clock signal ...." The operation code of claim 151 contains "precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed."

Conventional memory systems employing conventional DRAM devices, such as the one generally described in U.S. Patent 4,998,222, (hereinafter '222 patent), use asynchronous strobe signals to trigger, for example, a read operation (whether a normal or page mode type operation) in an asynchronous manner. Conventional DRAMs, upon detecting a falling edge transition of the strobe signal, latch the row address and sense a corresponding row using the sense amplifiers. In conventional DRAMs, precharging of the sense amplifiers occurs upon detection of a rising edge transition of the strobe signal (See, for example, the '222 patent, col. 2, lines 30-50). That is, *after* a read operation, conventional DRAMs perform the precharge function *only* in response

to additional instruction - typically transmitted via a rising edge transition of the strobe signal.

Thus, conventional DRAM devices, among other things, do not sample an operation code containing precharge information synchronously with respect to an external clock signal.[2] In addition, conventional DRAM devices do not automatically precharge a plurality of sense amplifiers (that is, precharge without further instruction), in response to the operation code, after the data is sensed. Instead, conventional DRAMs, perform precharging at the conclusion of a read operation *only* in response to further instruction[3] - typically transmitted to the memory device via the strobe signal. Therefore, for at least these reasons, claim 151 is not anticipated by conventional DRAM devices (i.e., the "admitted prior art" -- to the extent that phrase is understood).

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[2] The asynchronous strobe signals employed in the conventional DRAMs are not "external clock signal(s)" as described and claimed in the instant application. In this regard, notwithstanding the '222 patent's reference to certain asynchronous strobe signals as "input clock signals" (col. 1, lines 15-16 of the '222 patent), the "external clock signal" of the instant application is a *periodic signal* used to orchestrate the timing of events.

[3] While certain claims of the instant application are directed to a memory device that automatically precharges sense amplifiers after the data is sensed (from the array of memory cells), these remarks should in no way be interpreted as disclaiming or limiting the claims to memory devices responsive only to operation codes that include precharge information. Indeed, memory devices would fall within the scope of the claims of the instant application include those responsive to operation codes including precharge information and, for example: (1) operation codes not including precharge information and/or (2) operation codes indicative of a precharge command.

Claim 166 is not anticipated under USC 35 USC 102(a)

Claim 166 is directed to a synchronous integrated circuit memory device. Claim 166, in part, recites:

> a first input receiver to sample the first operation code bit in response to a first transition of the external clock signal;
>
> a second input receiver to sample a second operation code bit in response to the first transition of the external clock signal, wherein the second operation code bit indicates whether precharging the plurality of sense amplifiers occurs after the data has been sensed

For reasons similar to those set forth above with respect to claim 151, claim 166 is also not anticipated by conventional DRAM devices. For example, conventional DRAMs do not sample a first and second operation code bits in response to a transition of the external clock signal. Moreover, conventional DRAMs do not automatically precharge, in response to the second operation code bit, sense amplifiers after the data has been sensed. Rather, such conventional DRAMs respond to strobe signals in an asynchronous manner. Thus, for at least these reasons, claim 166 is not anticipated by conventional DRAMs i.e., "the admitted prior art" cited by the Examiner.

Claim 173 is not anticipated under USC 35 USC 102(a)

Claim 173 is directed to a method of operation of a synchronous integrated circuit memory device. Claim 173, in part, recites:

> sampling an operation code in response to a first transition of an external clock signal, wherein the operation code specifies a read operation and includes precharge information;
>
> automatically precharging the plurality of sense amplifiers in response to the precharge information, wherein the plurality of sense amplifiers is automatically precharged after the data is sensed

For reasons similar to those set forth above with respect to claim 151, claim 173 is also not anticipated by methods of operation of conventional DRAM devices. For example, conventional DRAMs do not sample an operation code in response to a transition of an external clock signal. Moreover, conventional DRAMs do not automatically precharge the plurality of sense amplifiers in response to the precharge information contained in an operation code. Rather, conventional DRAMs detect and respond to strobe signals (whenever those strobe signals are presented) in an asynchronous manner, to perform sensing and precharge operations. Thus, for at least these reasons, claim 173 is not anticipated by the conventional method of operation of conventional DRAMs, i.e., "the admitted prior art" cited by the Examiner.

Claim 182 is not anticipated under USC 35 USC 102(a)

Claim 182 is directed to a method of controlling a synchronous memory device. Claim 182, in part, recites:

> providing a first operation code to the memory device, wherein the first operation code indicates that the memory device ... precharge sense amplifiers used in reading the data from the memory cell array, wherein the sense amplifiers are precharged automatically after the data is read from the memory cell array...

For reasons similar to those set forth above with respect to claim 151, claim 182 is also not anticipated by methods of controlling conventional DRAM devices. For example, methods of controlling conventional DRAMs, do not include providing an operation code that indicates that the device automatically precharge sense amplifiers used in reading the data from the memory cell array, after the data is read from the array of memory cells. Rather, controlling conventional DRAMs involves the generation and holding of valid asynchronous strobe signals at specific times for the DRAM to perform sensing and precharge operations. Thus, for at least these reasons, claim 182 is not anticipated by the method of controlling conventional DRAM devices (as cited by the Examiner, i.e., "the admitted prior art".)

Information Disclosure Statement

Submitted concurrently herewith via First Class mail is an Information Disclosure Statement, and (modified) citation Form PTO-1449, along with a copy of each of the documents listed therein.

It is believed that the Examiner may find the above mentioned documents material to the patentability of one or more of the claims in the instant application. Accordingly, it is respectfully requested that the Examiner make his consideration formally of record with the next Action. As a courtesy to the Examiner, a copy of the Information Disclosure Statement and citation form PTO-1449 is attached hereto.

Conclusion

Applicants request reconsideration of the instant application in view of the foregoing remarks and amendments. Applicants submit that the pending claims present patentable subject matter. Accordingly, allowance of all of the claims is respectfully requested.

Respectfully submitted,

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Exhibit A -- Version with Markings to Show Changes Made

151. (Amended) A synchronous integrated circuit device having a memory array which includes dynamic random access memory cells, wherein the integrated circuit device comprises:

a clock receiver to receive an external clock signal;

a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic random access memory cells; and

a plurality of input receivers to sample an operation code synchronously with respect to [a transition of] the external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is automatically precharged after the data is sensed.

154. (Amended) The integrated circuit device of claim 152 [153] further including a delay lock loop, coupled to the plurality of output drivers, to synchronize the output of the first and second portions of the data with the external clock signal.

155. (Amended) The integrated circuit device of claim 152 [153] further including a plurality of multiplexers to provide the first and second portions of data to the plurality of output drivers, wherein each multiplexer of the plurality of multiplexers is coupled to [an] a respective output driver of the plurality of output drivers.

157. (Amended) The integrated circuit device of claim 151 wherein the plurality of input receivers further includes a first input receiver to sample a first bit of the operation code synchronously with respect to [the transition of] the external clock signal, wherein the precharge information is encoded in the

first bit of the operation code.

158. (Amended) The integrated circuit device of claim 157 wherein the plurality of input receivers further includes a second input receiver to sample a second bit of the operation code synchronously with respect to [the transition of] the external clock signal, wherein the second bit of the operation code specifies a read operation, wherein a portion of the data is output from the integrated circuit device in response to the second bit of the operation code specifying the read operation.

160. (Amended) The integrated circuit device of claim 151 wherein the operation code includes [a plurality of] bits that, [and wherein the plurality of bits,] in combination, encode[s] information which specifies that the plurality of sense amplifiers sense the data from the memory array.

164. (Amended) The integrated circuit device of claim 163 further including a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation, wherein the clock synchronization circuit is coupled to the plurality of output drivers to synchronize the output of the first and second portions of the data with the [internal] external clock signal.

165. (Amended) The integrated circuit device of claim 164 wherein the plurality of input receivers samples the operation code from a plurality of external signal lines of an external bus, wherein the external bus is used to carry, in a multiplexed format, the operation code, and the first and second portions of the data.

172. (Amended) The memory device of claim 166 further including:

row decoder circuitry, coupled to the array of memory cells,

to identify a row of the array of memory cells that stores the data to be sensed by the plurality of sense amplifiers; and

column decoder circuitry, coupled to the plurality of sense amplifiers [array of memory cells], to identify the portion of the data.

174. (Amended) The method of claim 173 further including sampling address information synchronously with respect to the external clock signal, wherein the address information identifies a location of the data within the array.

179. (Amended) The method of claim 178 further including identifying the data sensed in the plurality of sense amplifiers based on a second address portion.

181. (Amended) The method of claim 173 wherein outputting the data includes:

outputting a first portion of the data [is output] synchronously with respect to a rising edge transition of the external clock signal[,]; and

outputting a second portion of the data [is output] synchronously with respect to a falling edge transition of the external clock signal.

184. (Amended) The method of claim 182 further including providing a second operation code to the memory device, wherein the second operation code instructs the memory device to:

receive input data to be written to the memory cell array;

write the input data to the memory cell array using sense amplifiers of the plurality of sense amplifiers; and

precharge the sense amplifiers used in writing the input data

to the memory cell array, wherein the sense amplifiers are precharged automatically after the input data is written to the memory cell array.

186. (Amended) The method of claim 182 further including:

providing, to the memory device, a row address [and a column address]; and

providing a second operation code to the memory device, wherein the second operation code includes [a plurality of bits, wherein the plurality of] bits that, in combination, encode[s] information which indicates that the memory device sense data from a specified location of the memory cell array using at least a portion of the plurality of sense amplifiers, wherein the specified location is identified by the row address [and the column address].

189. (Amended) A synchronous memory device having a memory array which includes dynamic memory cells, wherein the memory device comprises:

a plurality of sense amplifiers, coupled to the memory array, to sense data from the dynamic memory cells; [and]

a plurality of input receivers to sample an operation code synchronously with respect to [a transition of] an external clock signal, the operation code including precharge information, wherein, in response to the precharge information, the plurality of sense amplifiers is [are] automatically precharged after the data is sensed;

a plurality of output drivers to output first and second portions of the data in response to the operation code specifying a read operation; and

a delay locked loop, coupled to the plurality of output drivers, to synchronize the output of the first and second portions of the data with the external clock signal.

191. (Amended) The memory device of claim 189 further including a plurality of multiplexers, wherein each multiplexer of the plurality of multiplexers is coupled to a[n] respective output driver of the plurality of output drivers.

192. (Amended) The memory device of claim 191 wherein the plurality of multiplexers provides the first portion of the data to the plurality of output drivers in response to a rising edge transition of the external clock signal, and wherein the plurality of multiplexers provides the second portion of the data to the plurality of output drivers in response to a falling edge transition of the external clock signal.

193. (Amended) The memory device of claim 189 wherein the plurality of input receivers further includes a first input receiver to sample a first bit of the operation code synchronously with respect to [the transition of] the external clock signal, wherein the precharge information is encoded in the first bit of the operation code.

194. (Amended) The memory device of claim 193 wherein the plurality of input receivers further includes a second input receiver to sample a second bit of the operation code synchronously with respect to [the transition of] the external clock signal, wherein an encoding of the second bit of the operation code specifies the read operation.

195. (Amended) The memory device of claim 189 wherein the delay locked loop includes:

a delay line to generate an internal clock signal, wherein the internal clock signal has a delay with respect to the external clock signal; and

a comparator to compare the internal clock signal with the

external clock signal, wherein the delay of the internal clock signal is adjusted based on the comparison between the internal clock signal and the external clock signal, wherein the output of the first and second portions of the data is synchronized with the external clock signal using the internal clock signal.